Hot-Carrier Reliability of Transistors Fabricated by a 0.25-μm Fully-Depleted SOI CMOS Process

Udo Lieneweg and Anne Vandooren

Jet Propulsion Laboratory / California Institute of Technology
Mailstop 300-315, Pasadena CA 91109
818-354-3444, Udo.Lieneweg@jpl.nasa.gov

Abstract

Fully depleted (FD) Silicon-On-Insulator (SOI) transistors are particularly susceptible to hot carrier effects because the thin silicon body has two closely spaced, interacting oxide interfaces. In the present work, the hot-carrier degradation of transistors fabricated by a 0.25-μm FD SOI CMOS process was investigated. The degradation of key transistor parameters under drain voltage stress and worst-case gate bias was observed as a function of time. The shift of the front and back threshold voltages was analysed with different back biases in order to separate front and back (buried) oxide degradation. A lifetime defined by a front threshold voltage shift equal to one sigma of the original distribution was extracted as function of the drain voltage. Whereas the first batch of transistors showed a large sigma but a reasonable lifetime at 2 Volt, the other had a reasonable sigma but a lifetime of only 1 day at that voltage. Even when comparing equal absolute degradation, the lifetime of the second batch was much inferior. It is shown that in the second case the short lifetime is caused by poor properties of the buried oxide (here created by a SIMOX process). Therefore, SOI wafers must be characterized for their hot-carrier susceptibility.

Samples

The samples were obtained as process monitor chips from MIT/Lincoln Laboratory. The process parameters are listed in Table 1. Three-terminal, floating body transistors of various gate lengths L and widths W were found on the chip. The first batch of chips was received in October 1999, the second one in April 2000.

Table 1: Process parameters

Parameter	Value
Gate oxide thickness	7.3 nm
Silicon film thickness	50 nm
Buried oxide thickness	195 nm
Wafer type	SIMOX
Isolation technology	mesa-etched
Minimum gate length (target)	250 nm
Sidewall oxide thickness	15 nm
n-channel doping	$4\times10^{17}cm^{-3}$
p-channel doping	$4\times10^{17}cm^{-3}$

Current-Voltage Characteristics

Figure 1 shows drain current - front voltage characteristics of transistors from the two batches. Batch 2 exhibits a much tighter threshold voltage control with σ = 25 mV than batch 1 with σ = 290 mV.

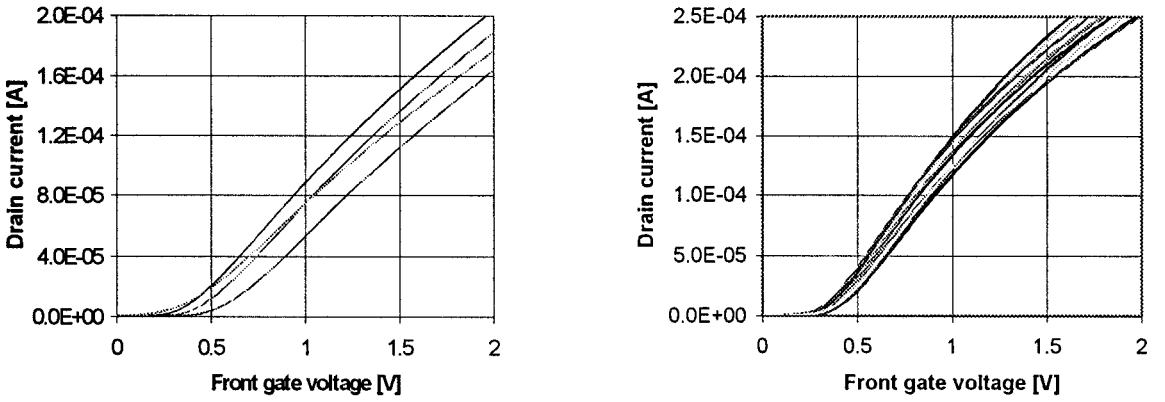

Figure 1: Id vs Vgs characteristics of L/W = 0.25-μm/8-μm NMOS transistors: (a) 4 transistors at Vd=100 mV from different chips of batch 1, (b) 10 transistors at Vd = 50 mV from different chips of batch 2.

Hot-Carrier Stress

Transistors were stressed with a drain voltage $V_{d,stress}$ while the front gate voltage was kept at $V_{d,stress}/2$. Figure 2 shows an example of the induced threshold voltage shift.

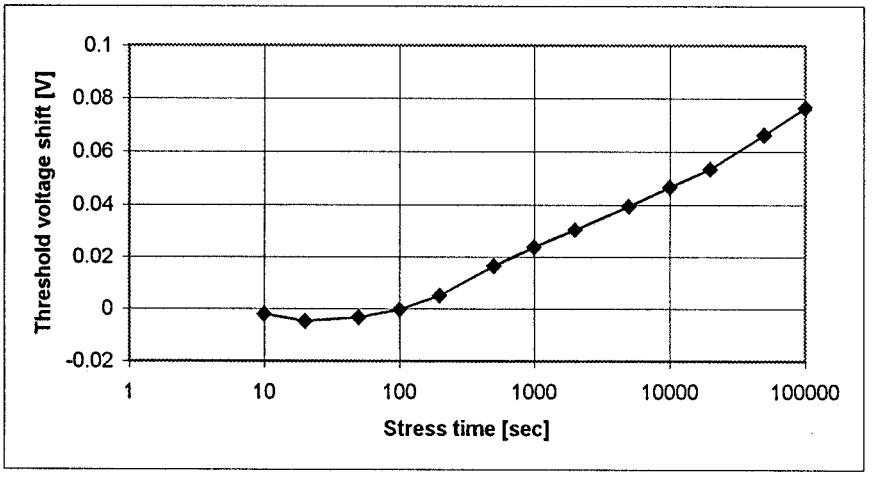

Figure 2: Threshold voltage shift versus stress time in a 0.25-μm NMOS device from batch 1 at $V_{d,stress}$ = 2.5 V, $V_{g,stress}$ = 1.25 V, and $V_{g2,stress}$ = 0 V

A lifetime τ is defined as the stress time at which a certain threshold voltage shift is produced. Lifetimes for samples from batch 1 are shown in Figure 3. The data have been fitted with lines following

$$\tau = \tau_0 \exp (V_0 / V_d),$$

where τ_0 and V_0 are scaling factors. Data from stress voltages larger than 2.75 V show a smaller V_0 due to a different degradation mechanism. Extrapolation shows that at an operating voltage of 2 V the 100-mV lifetime of 0.25-μm NMOSFETs exceeds 10,000 days or 30 years. In comparison to that the 10-mV lifetime of 0.30-μm NMOSFETs is only about 1 year. Operation of the latter at 1.8 V would extend the 10-mV lifetime to 30 years again. However, compared to the standard deviation of threshold voltages in unstressed devices of already 290 mV, a change of 10-mV seems to be inconsequential and error-prone.

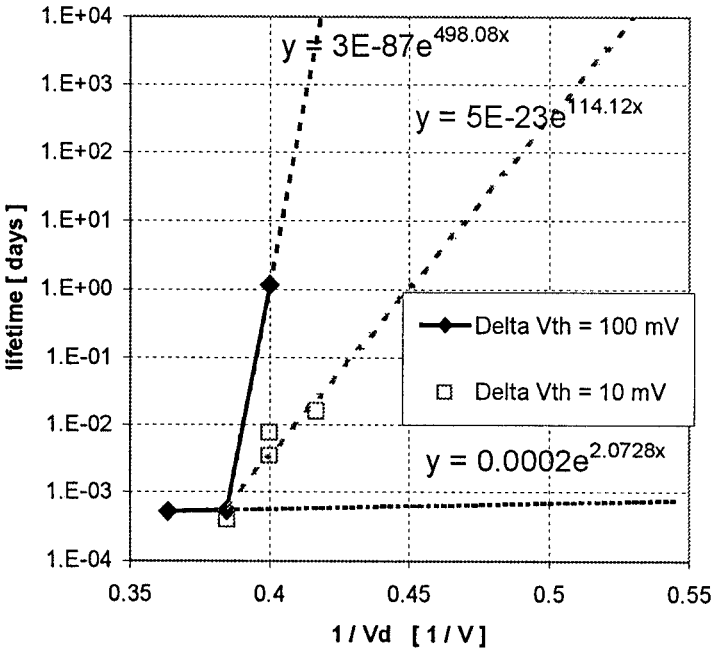

Figure 3: Threshold-voltage lifetime vs. reciprocal stress drain voltage for NMOS samples from batch 1. Filled symbols: L = 0.25 μm, ΔVth = 100 mV; open symbols L= 0.30 μm, ΔVth = 10 mV

The front threshold voltage shifts of samples from batch 2 are shown in Figure 4. In comparison to the data obtained from batch 1, these samples degrade much faster. At a drain voltage of 2.0 V, a 10-mV shift is obtained at less than 10 hours and a shift equal to σ= 25 mV in less than 4 days. When the threshold voltages were measured with –30 V applied between substrate and source, the shifts after stress at 2.0 V are almost zero and the ones at 2.2 V greatly reduced. Since the substrate acts through the buried oxide as a backgate, a negative bias brings the backside of the p-type silicon body into accumulation. This shields any charge created in the buried oxide or at its interface with the body during stress. The conclusion is that, in the samples of batch 2, the buried

oxide is affected by hot carrier injection from the front channel. Therefore, SOI wafers must be screened for their hot-carrier susceptibility.

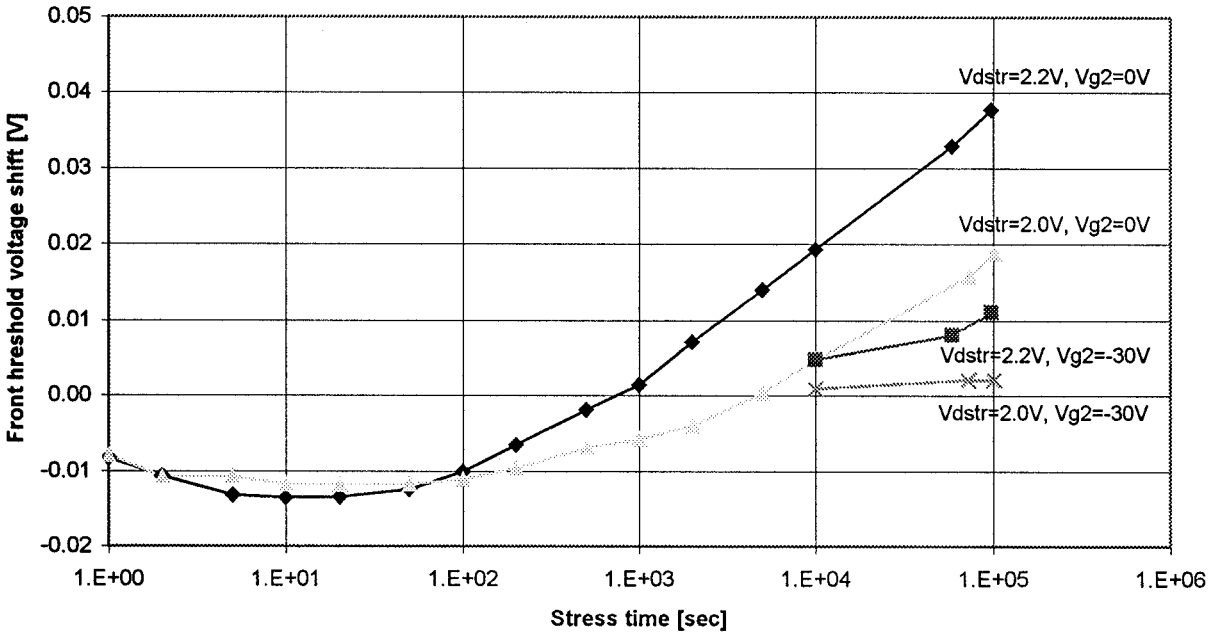

Figure 4: Front threshold voltage shift in 0.25-μm/20-μm NMOSFETs from batch 2, measured with backgate voltages Vg2 = 0 V and –30 V, versus time stressed at Vdstr = 2 V and 2.2V

Acknowledgments

This research was carried out at the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration with funding by the NASA Electronic Parts Program. We wish to thank Distinguished Visiting Professor S. Cristoloveanu for many valuable comments and members of the Reliability Laboratory for their assistance. The samples were obtained from MIT/Lincoln Laboratory through the Deep Space One Program.